Scientific Publications

Dr. Stephan Henzler, August 31, 2009

1. M. Weis, A. Pfizner, D. Kasprowicz, R. Emling, T. Fischer, S. Henzler, W. Maly, and D. Schmitt-Landsiedel, "Stacked 3-Dimensional 6T SRAM Cell with Independent Double Gate Transistors," in *International Conference on Integrated Circuit Design and Technology (ICICDT)*, 2009.
2. M. Eireiner, D. Schmitt-Landsiedel, P. Wallner, A. Schoene, and S. Henzler, "Adaptive Circuit Block Model for Power Supply Noise Analysis of Low Power System-on-Chip," in *International Symposium on System-on-Chip*, 2009.
3. S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "A Local Passive Interpolation Concept for Variation Tolerant High Resolution Time-to-Digital Conversion," *Journal of Solid State Circuits*, vol. 43/7, pp. 1666–1676, 7/2008.
4. S. Henzler and S. Koeppe, "Design and Application of Power Optimized High-Speed CMOS Frequency Dividers," *Transactions on Very Large Scale Integration Systems*, vol. 16/11, pp. 1513–1520, 11/2008.
5. S. Henzler, S. Koeppe, W. Kamp, H. Mulatz, and D. Schmitt-Landsiedel, "90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization," in *International Solid State Circuits Conference (ISSCC)*, 2008.
6. S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, "Variation Tolerant High Resolution and Low-Latency Time-to-Digital Converter," in *European Solid State Circuits Conference (ESSCIRC)*, 2007.
7. M. Eireiner, S. Henzler, G. Georgakos, J. Berthold, and D. Schmitt-Landsiedel, "In-Situ Delay Characterization and Local Supply Voltage Adjustment for Compensation of Local Parametric Variations," *Journal of Solid State Circuits (JSSC)*, vol. 42/7, no. 7, pp. 1583–1592, 2007.
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9. M. Eireiner, S. Henzler, X. Zhang, J. Berthold, and Schmitt-Landsiedel. D., "Impact of On-Chip Inductance on Power Supply Integrity," *Advances in Radio Science, URSI Kleinheubacher Berichte*, vol. 6, 2007.
10. S. Henzler, *Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies*, Number ISBN 1-4020-5080-1 in Springer Series in Advanced Microelectronics. Springer Verlag, 10/2006.

11. S. Henzler, *Power Management of Digital Circuits in Deep Sub-Micron CMOS Technologies*, Dissertation, Technische Universitaet Muenchen, 10/2006.
12. T. Nirschl, S. Henzler, J. Fischer, B. Fulde, A. Bargagli-Stoffi, M. Sterkel, J. Sedlmeir, C. Weber, R. Heinrich, U. Schaper, J. Einfeld, R. Neubert, U. Feldmann, K. Stahrenberg, E. Ruderer, G. Georgakos, A. Huber, R. Kakoschke, W. Hansch, and D. Schmitt-Landsiedel, "Scaling Properties of the Tunneling Field Effect Transistor (TFET): Device and Circuit," *Solid State Electronics*, vol. 50, pp. 44–51, 2006.
13. S. Henzler, M. Eireiner, J. Berthold, G. Georgakos, and D. Schmitt-Landsiedel, "Activation Technique for Sleep-Transistor Circuits for Reduced Power Supply Noise," in *European Solid State Circuits Conference (ESSCIRC)*, 9/2006.
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15. M. Eireiner, S. Henzler, T. Missal, J. Berthold, and D. Schmitt-Landsiedel, "Power Supply Network Design: A Case Study Driven Approach," *Advances in Radio Science, URSI Kleinheubacher Berichte*, vol. 5, pp. 279–284, 2006.
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17. S. Henzler, G. Georgakos, M. Eireiner, T. Nirschl, Pacha. C., J. Berthold, and D. Schmitt-Landsiedel, "Dynamic State Retention Flip-Flop for Fine-Grained Power Gating With Small Design and Power Overhead," *Journal of Solid State Circuits (JSSC)*, vol. 41/7, pp. 1654–1661, 7/2006.
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