Technical Presentations

Dr. Stephan Henzler, August 31, 2009

1. "Robust High-Resolution Time-to-Digital Converters -A Short Overview," Joint NTU-TUM Workshop 2009 (invited), 28.4.2009.
2. "High Resolution Time-to-Digital Converters," Nanyang Technological University, Singapore (invited tutorial), 2/2008.
3. "A Tutorial on Robust High Resolution Time-to-Digital Converter," Kleinheubacher Tagung (invited tutorial), 2008.
4. "90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization," presented at *International Solid State Circuits Conference (ISSCC)*, 2008.
5. "Variation Tolerant High Resolution and Low-Latency Time-to-Digital Converter," presented at *European Solid State Circuits Conference (ESSCIRC)*, 2007.
6. "Entwurf Digitaler High-Speed CMOS Schaltungen," Seminar Elektronische Bauelemente, Technische Universitaet Muenchen, 1/2007.
7. "Elektronik mit Nanometer-Transistoren, Herausforderung und Chance fuer kreatives Schaltungsdesign," Festkolloquium Entwicklungen und Trends in der Mikroelektronik, 10/2006.
8. "Activation Technique for Sleep-Transistor Circuits for Reduced Power Supply Noise," presented at *European Solid State Circuits Conference (ESSCIRC)*, 9/2006.
9. "High-Speed Low-Power Frequency Divider With Intrinsic Phase Rotator," presented at *International Symposium on Low-Power Electronics and Design (ISLPED)*, 10/2006.
10. "Power Gating Techniques for Low Stand-By Power Consumption," Nanyang Technological University, Singapore, 3/2006.
11. "Power Gating Techniques for Low Stand-By Power Consumption," Infineon Technologies, Singapore, 3/2006.
12. "Dynamic State Retention FlipFlop for Fine-Grained Sleep Transistor Scheme," presented at *European Solid State Circuits Conference (ESSCIRC)*, 9/2005.
13. "Implementation Challenges of Power Gating (invited tutorial)," Kleinheubacher Tagung, 2005.
14. "Design and Technology of Fine-Grained Sleep Transistor Circuits in Ultra-Deep Sub-Micron CMOS Technologies (invited paper)," presented at *International Conference on Integrated Circuit Design and Technology (ICICDT)*, 5/2005.
15. "Making Adiabatic Circuits Attractive for Todays VLSI Industry by Multi-Mode Operation," presented at *Computing Frontiers*, 5/2005.
16. "Sleep Transistor Circuits for Fine-Grained Power Switch-Off with Short Power-Down Times," presented at *Internatonal Solid State Circuits Conference (ISSCC)*, 2/2005.
17. "Impact of Level-Converter on Power-Saving Capability of Clustered Voltage Scaling," Kleinheubacher Tagung, 2004.

18. "Single Supply Voltage High-Speed Semi-Dynamic Level-Converting FlipFlop with Low Power and Area Consumption," presented at *International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)*, 9/2004.
19. "Two Level Compact Simulation Methodology for Timing Analysis Of Power-Switched Circuits," presented at *International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)*, 9/2004.
20. "Theory of Circuit Block Switch-Off Schemes," Kleinheubacher Tagung, 2004.
21. "Digital Low-Power CMOS Design Styles," Low-Power Community, Infineon Technologies, Munich, 8/2004.
22. "Digitale Low-Power CMOS Schaltungstechniken," Corporate Logic, Infineon Technologies,, 1/2004.
23. "Design Aspects and Technological Scaling Limits of ZigZag Circuit Block Swith-Off Schemes," presented at *International Conference on Very Large Scale Integration of System on Chip (VLSI-SOC)*, 12/2003.