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Integrated Circuits Design Lab II
Analog and Power Management

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Lab Introduction

This lab gives an opportunity for students to more deeply study power design theory and develop an analog circuit on their own. This handout explains which circuits have to be realized, illustrates the main steps to design it, and gives the requirements that the circuit must fulfill. The students must then design a circuit/system, that operates according to the indicated functionality, dimension it to meet the given requirements, and then characterize it through simulation. Since the design of a circuit is usually much more complex than its analysis, from theoretical courses, and since it gives many more degrees of freedom, the students are encouraged to come to discuss their difficulties and they must report their progresses along the semester.
Due to the time constraints the full custom layout step is omitted. For all tasks, a suitable mixture of hand calculations and transistor level simulations are mandantory to to meet the specifications. The 'brute force' approach will not lead to a satisfactory design in time.

There are 2 LABs which you can select from:

1. Single-Ended Operational Transconductance Amplifier:
   In this LAB, you are requested to design a single-ended OTA following a given specification. The challange of this task is the selection of the right topology to achieve the high gain specification. We recommend this LAB to students, who want to design a highly optimized amplifier and exhaust the given technology.

2. Voltage Reference Circuit:
   The design provides an opportunity for students to perform a highly stable voltage reference circuit. The circuitry requires a proper dimensioning of the temperature compensating core as well as an amplifier as control unit. We recommend this LAB to students, who are interested in device physics, amplifier as well as feedback control design.

Rules and Suggestions in the Labs:

1. **Deliverables**:
   - A "Design Report" comprising of three parts should be handed in. It should be properly formatted (*e.g.* written in LaTeX or a properly formatted Word document.) The first part should be completed by **May 12**, the second part **June 12**, and the last part **August 31**. The report should be written assuming the reader has taken a Mixed-Signal course, but is not necessarily an expert.
   - A **15 minute** presentation will take place on **July 23**, where each group shows their outcomes up to that point.
   - Your Simulink model, any MATLAB scripts used, your HDL code (if applicable), and the Cadence schematics and ADE states used to simulate your results. These should be delivered when the relevent section of the report is due.
2. **Teamwork**: Each topic has two or three participants. Please make sure you are in good relationship and achieve the final goal together. The division of labour is determined by each group themselves.
3. **Lab usage**: The lab room (N4303) is open Monday to Friday during office hours (8:00 - 19:00). These computers can also be accessed from any Linux machine on the LRZ network via SSH from the using the command `ssh -X [groupname]@[ip-address]` where `groupname` is the groupname given to you and `ip-address` is one of the ip addresses printed on the lab computers. Since another group might also using the same machine remotely, please do not shutdown the computer, just log off. For security purposes, these machines will not read USB drives.
4. **Grading**: The three reports and the final presentation are graded, not only in terms of its content, but also considering their quality and clarity.

References

[1] E. Allen and D. Holberg, *CMOS Analog Circuit Design.* New York, Oxford University Press, 2002.

Single-Ended OTA

Specifications The objective of this project is to design an Operational Transconductance Amplifier (OTA) with differential input and single ended output. The amplifier

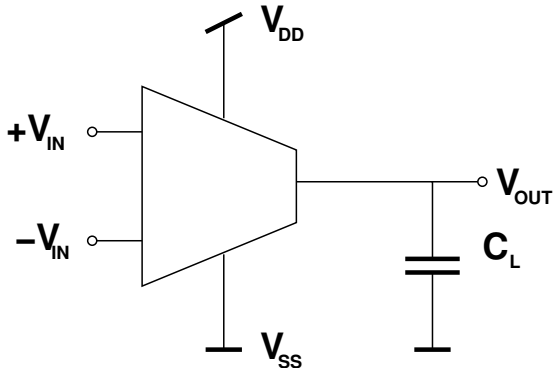

Figure 1: Differential amplifier with capacitive load

must meet the given specifications:

Specifications	**Condition**	**Note**
V_{DD}	1.8V	positive supply voltage
V_{SS}	0V	negative supply voltage
C_L	3pF	load capacitance
A_{DM}	$\geq$ 90dB	DC small signal differential mode voltage gain
CMRR $= A_{DM}/A_{CM}$	$\geq$ 80dB	common mode rejection ratio
PSRR	$\geq$ 80dB	power supply rejection ratio
GBW	$\geq$ 10MHz	gain bandwidth, i.e. unity gain frequency
PM	$\geq 55°$	phase margin
SR	$\geq 30V/\mu S$	slew rate
$V_{out,pp}$	1V	output voltage range
V_{ICM}	0.9V	common mode input voltage
P	minimize	

The design goal is to minimize the power consumption of the amplifier.

Parameter Extraction

1. The first step is to extract the level 1 parameters of the devices you will be working with so you can make accurate calculations. Each extraction should be done for both the pMOS and the nMOS for at least these three different channel lengths, L_{min},$2 \cdot L_{min}$, and $5 \cdot L_{min}$.

   (a) Extract the threshold voltage V_T. As a first approximation, V_T is defined as: $V_{GS}@I_{DS} = 300\text{nA}\cdot(W/L)$, $V_{DS} = V_{DD}/2$ for the **nMOS** and $V_{GS}@I_{DS} = -70\text{nA}\cdot(W/L)$, $V_{DS} = -V_{DD}/2$ for the **pMOS**.

   (b) Extract μC_{ox}. this calculation is explained in [1]

   (c) Extract λ. this calculation is also shown in [1]

   (d) Compare the simulated transistor characteristics to your own model.

(Finish above problems before May 12 and submit the report together with any code to your supervisor. Be sure to discuss the results with your supervisor before this deadline!

If your model does not fit the simulated curves, think about improvements in your algorithm to extract V_T, μC_{ox} and λ! Also think about which V_{GS} and V_{DS} values make sense for the parameter extraction.

Topology

1. A topology needs to be selected that can meet the specifications listed above. You can select most any topology as long as it meets the specifications and is applicable to this technology node.

   (a) Estimate the value for each of the specifications in your circuit.

   (b) For the specific topology you have selected, explain why you selected it.

(Finish above problems before June 12 and submit the report together with the codes and simulation results to your supervisor)
Implementation and Testing

1. You will now implement your topology in Cadence Virtuoso. Ideal sources (VDC and VSOURCE from "basic" lib.) can only be used to generate the supply voltages, not to generate bias currents or voltages. The passive devices from the "analogLib" (capacitor = cap, resistor = res) should be used. For any OpAmp in your design, you should use a simple 2-stage Miller OpAmp implementation. When you have verified the circuit is working properly, make the following open loop analyses:

(a) what is the open loop gain (A_{DM}) of the circuit?

(b) What is the common mode rejection ratio (CMRR) of the circuit?

(c) What is the power supply rejection ratio (PSRR) of your circuit?

(d) Determine the Gain-Bandwidth product and the phase margin of your circuit.

(e) Determine the input refered noise: $\left(\sqrt{\int_{1k}^{10g} (\text{output noise})^2 df}\right) / A_{DM}$

Now perform these other analyses as well:

(f) Settling time: input voltage step $V_{in} = V_{CM}$-0.5V $\rightarrow V_{CM}$+0.5V, $V_{out} = V_{in} \pm 5\%$

(g) Slew rate: input voltage step $V_{in} = V_{CM} - 0.5V \rightarrow V_{CM} + 0.5V$, slew rate measured between $V_{out} = 0.1 \cdot V_{out,low}$ and $0.9 \cdot V_{out,high}$

(h) Transient response: V_{in} =0.5V$\cdot \sin(2\pi \cdot 5\text{MHz} \cdot t)$ (Transient Analysis)

(i) Output voltage range: $V_{in} = V_{DD}/2 \cdot \sin(2\pi \cdot 1\text{kHz} \cdot t)$ (Transient Analysis)

(j) Harmonic distortion: V_{in} =0.5V$\cdot \sin(2\pi \cdot 5\text{MHz} \cdot t)$ (Periodic Steady State Analysis)

(Finish above problems before August 31 and submit the report together with the codes and simulation results to your supervisor)

Please save the settings for for all of the simulations you use for your report! Go to *Session→Save State...*, then select *Cellview* at the top of the dialog. Then under *Cellview Options* give a meaningful name for *State* and a brief description of the test under *Description*.