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Mixed-Signal IC Design LAB

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LAB Introduction

There are 3 Labs to choose from:

1. 1^{st} **Order 1-Bit $\Sigma\Delta$-ADC for Audio Applications**:
   In this lab, you will design a 1^{st} order $\Sigma\Delta$-ADC able to process signals for voice applications from system level to circuit level. This lab will have an emphasis on signal processing and system level design.

2. **Algorithmic ADC for Sensor Applications**:
   In this lab, you will design an algorithmic ADC following a given specification from system level to circuit level. This lab will have an emphasis on designing with switched-cap circuits and the transistor-level design.

3. **Successive Approximation ADC for Sensor Applications**:
   In this lab, you will design a sucessive approximation ADC following a given specification from system level to circuit level. This lab will have an emphasis on using different Cadence tools throughout the entire design process. The control logic for this ADC will be implemented with either Verilog or VHDL.

Rules and Suggestions in the Labs:

1. **Deliverables**:
   - A "Design Report" comprising of three parts should be handed in. It should be properly formatted (*e.g.* written in LaTeX or a properly formatted Word document.) The first part should be completed by **May 12**, the second part **June 12**, and the last part **August 31**. The report should be written assuming the reader has taken a Mixed-Signal course, but is not necessarily an expert.
   - A **15 minute** presentation will take place on **Late July**, where each group shows their outcomes up to that point.
   - Your Simulink model, any MATLAB scripts used, your HDL code (if applicable), and the Cadence schematics and ADE states used to simulate your results. These should be delivered when the relevent section of the report is due.
2. **Teamwork**: Each topic has two or three participants. Please make sure you are in good relationship and achieve the final goal together. The division of labour is determined by each group themselves.
3. **Lab usage**: The lab room (N4303) is open Monday to Friday during office hours (8:00 - 19:00). These computers can also be accessed from any Linux machine on the LRZ network via SSH from the using the command `ssh -X [groupname]@[ip-address]` where `groupname` is the groupname given to you and `ip-address` is one of the ip addresses printed on the lab computers. Since another group might also using the same machine remotely, please do not shutdown the computer, just log off. For security purposes, these machines will not read USB drives.
4. **Grading**: The three reports and the final presentation are graded, not only in terms of its content, but also considering their quality and clarity.

Reference Books

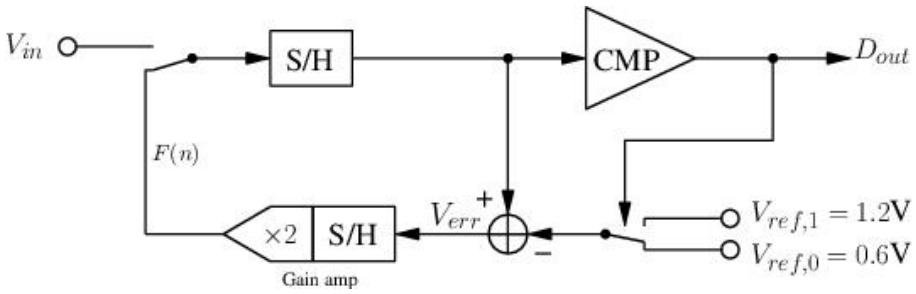
- D.A. Johns; K. Martin, Analog Integrated Circuit Design, Wiley, 1997
- B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001
- R. Schreier; G.C. Temes, Understanding Delta-Sigma Data Converters, IEEE Press, 2005
- S.R. Norsworthy; R. Schreier, Delta-Sigma Data Converters, IEEE Press, 1997
- A.V. Oppenheim; A.S. Willsky, Signals and Systems, Prentice Hall, 1999
- R.J. Baker; H.W. Li; D.E. Boyce, CMOS, Circuit Design, Layout and Simulation, Wiley, 1997
- R. Gregorian; G.C. Temes, Analog MOS Integrated Circuits For Signal Processing, Wiley, 1986
- S.J. Orfanidis, Introduction to Signal Processing, Prentice Hall, 1998

Algorithmic ADC

Specifications In this lab, a 10-bit algorithmic ADC will be designed to sample and convert a slow analog signal coming in from a sensor. The specifications are given as follows:

Input voltage range	?? (TBD)
Input frequency range	0-20kHz
Supply voltage (V_{dd})	1.8V
Ground voltage (V_{gnd})	0V
Reference voltage (V_{ref})	0.6V, 1.2V
Required SNR	$>$ 60dB

The system architecture of a typical algorithmic ADC is shown below:



Problems for system design

1. Concept and Theories

   (a) What is the basic principle of an algorithmic ADC?

   (b) What is the residue voltage? What range does a residue voltage stay in an algorithmic ADC? What happens if the residue voltage goes beyond this range?

   (c) What is the relationship between the residue voltage and the input voltage? What happens if the input voltage is out of the input voltage range?

   (d) How many cycles does the algorithmic ADC need for one conversion?

   (e) When the plot V_{out} *vs.* V_{in} (a Robertson diagram) is drawn, what characteristic of the plot do you expect to see, why?

2. Spectrum analysis

   (a) What is the Discrete Fourier Transform? What is the equation that defines it?

   (b) MATLAB does not provide a `DFT()` function; instead it provides the similar function `FFT()`. What is the relationship between these two functions?

   (c) Briefly explain what a 'window function' is. Why is it used and how does it affect the results?

   (d) How is the SNR of a sinusoidal input calculated from the DFT? Write a MATLAB function to calculate this.

   (Finish above problems before May 12 and submit the report to your supervisor)

3. Specification related

   (a) Given the two reference voltages above, determine the input voltage range.

   (b) Determine the required number of cycles corresponding to one conversion and sampling frequency f_s according to the given specification.

   (c) Prototype the behavioural model for the algorithmic ADC using Simulink.

   (d) Draw the Robertson diagram showing the conversion process of your prototype when a constant, DC input is applied.

   (e) Add gain error to the $\times 2$ block. Draw the Robertson plot again. What happens this time? What about a negative gain error?

   (f) Plot the output spectrum for a periodical sinusoidal input voltage. How much is the noise floor below the input signal? Compare the simulated SNR to your SNR calculations.

   (Finish above problems before June 12 and submit the report together with the codes and simulation results your supervisor)

Problems for circuit design

4. You will now implement your Simulink prototype in Cadence Virtuoso in two iterations. In the first iteration, you will create an circuit using (mostly) ideal components. Then you will replace these ideal components with transistors for a more realistic circuit. Please implement your design using a switched-capacitor approach.

   (a) Based on your Simulink model, how can you split up your design into managable blocks? Create a cell for each of these blocks as well as a cell for an ideal switch. How can you verify that each of these blocks are properly functioning?

   (b) The thermal noise of a capacitor will set a limit on the sampling capacitance for a switched-cap circuit. Determine the minimum required sampling capacitance C_s so that the RMS noise is less than $\frac{1}{2}$LSB.

   (c) Switched capacitor circuits are usually clocked with two alternating phases Φ_1 and Φ_2. How are these clocks generated and why is it not a good idea to use just one clock signal and an inverter?

   Verify that the circuit behaviour is correct using the same input signals used in your Simulink model.

Cadence's default settings for transient simulations can create excessive data and long simulation times. Set the `strobeperiod` and `strobedelay` parameters to more sensible values, if needed. You can find these settings in the transient simulation settings by pressing *Options...* then navigating to the *Output* tab.

5. Once the circuit works with ideal components, work on the "transistor-level" implementation. In this iteration, you should replace the ideal components with more realistic components. You should also use non-ideal OpAmps; however, a transistor-level description is not necessary: adjusting the cell parameters to more realistic values is sufficient.

   (a) What non-ideal behaviour is introduced by using transistors instead of ideal switches? Which type of switch (NMOS, transmission gate, *etc*...) is best suited for this ADC?

   (b) How does a finite gain of a real OpAmp affect the result? Calculate the minimum DC-gain for the OpAmp to ensure an error of less than $\frac{1}{2}$LSB (ignoring the thermal noise and finite bandwidth).

   (c) How does a finite bandwidth affect the result? Calculate the required bandwidth for the OpAmps so the settling error over is less than $\frac{1}{2}$LSB (ignoring the finite gain and the thermal noise).

   Apply the same input signals as before to your circuit. Compare these results to your Simulink results. What is the final SNR of your circuit and where is the source of this noise?

Please save the settings for for all of the simulations you use for your report! Go to *Session→Save State...*, then select *Cellview* at the top of the dialog. Then under *Cellview Options* give a meaningful name for *State* and a brief description of the test under *Description*.

(Finish above problems before August 31 and submit the report together with the simulation files and results to your supervisor)