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Integrated Circuits Design Lab II
Analog and Power Management

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Lab Introduction

This activity is meant for those students who wants to deepen their knowledge in the field of power electronics. More precisely both projects deal with DC-DC converters. The first task is focused on the analysis process and the dimensioning of the components to carry out a complete design while the second one wants to give an opportunity to the students to develop an analog circuit on their own. Anyhow, the students must therefore design a circuit/system, that operates according to the indicated functionality, opportunely dimension it to meet the given requirements, and then characterize it through computer simulations. This handout explains which circuits has to be realized, illustrates the main steps to design it and gives the requirements that the circuit must fulfill. Since the treated topics are quite complex, the students are encouraged to come to discuss their difficulties and they must report their progresses along the semester. ***There is 1 lab which you can select from:***

1. Switched-mode Converter circuit:
   The purpose of this LAB is to show the fundamental steps of the design of a switched-mode power supply. The students will have to face several issues related to the proper choice and design of the topology following a given specification. Then they need to dimension the compensation network to obtain a working design. We recommend this LAB to students, who want to deepen the switched-mode power supply topic and gain experience in the design process of the converters.

Rules and Suggestions in the Labs:

1. **Deliverables**:
   - A "Design Report" comprising of three parts should be handed in. It should be properly formatted (*e.g.* written in LaTeX or a properly formatted Word document.) The first part should be completed by **May 12**, the second part **June 12**, and the last part **August 31**. The report should be written assuming the reader has taken a Mixed-Signal course, but is not necessarily an expert.
   - A **15 minute** presentation will take place on **Late July**, where each group shows their outcomes up to that point.
   - Your Simulink model, any MATLAB scripts used, your HDL code (if applicable), and the Cadence schematics and ADE states used to simulate your results. These should be delivered when the relevent section of the report is due.
2. **Teamwork**: Each topic has two or three participants. Please make sure you are in good relationship and achieve the final goal together. The division of labour is determined by each group themselves.
3. **Lab usage**: The lab room (N4303) is open Monday to Friday during office hours (8:00 - 19:00). These computers can also be accessed from any Linux machine on the LRZ network via SSH from the using the command `ssh -X [groupname]@[ip-address]` where `groupname` is the groupname given to you and `ip-address` is one of the ip addresses printed on the lab computers. Since another group might also using the same machine remotely, please do not shutdown the computer, just log off. For security purposes, these machines will not read USB drives.
4. **Grading**: The three reports and the final presentation are graded, not only in terms of its content, but also considering their quality and clarity.

References

[1] E. Allen and D. Holberg, *CMOS Analog Circuit Design.* New York, Oxford University Press, 2002.

Switched-mode Converter

Specifications The objective of this project is to design a square wave switched-mode power converter

The converter must meet the following specifications:

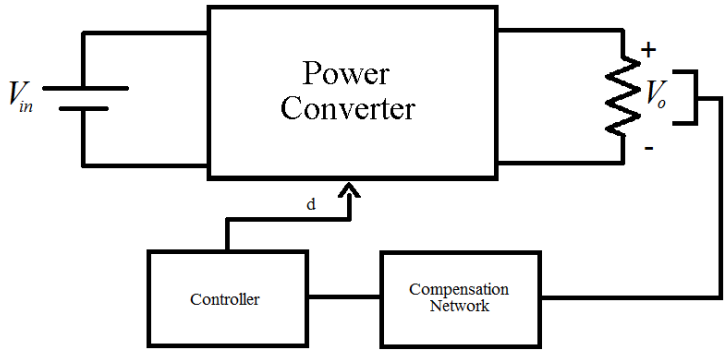

Figure 1: Simplified block scheme of a power converter

Specification	**Condition**	**Note**
V_O	1.8V	output voltage
I_{O_MIN}	500mA	minimum load current
I_{O_MAX}	2A	maximum load current
V_{IN_MIN}	3.3V	minimum input voltage
V_{IN_MAX}	5V	maximum input voltage
V_{O_ripple}	40mV	maximum admitted ripple voltage
Isolation	Not Req.	galvanic isolation
f_{SW}	200kHz	switching frequency
V_{REF}	1V	reference voltage available
Efficiency	$\geq 70\%$	required efficiency
Cost	minimize	cost of the implementation

The design goal is to find the proper trade-off between requirements and costs with a reliable result.

Understanding the Specifications

1. Take into account all of the specifications

   (a) Decide on the topology to use and justify it. Draw the schematic for this topology.

   (b) Which conduction mode makes more sense for this converter. Why?

   (c) Choose the control technique for the converter. Why did you choose this converter?

   Be sure to discuss your results with your supervisor before handing in your report!

(Finish above problems before May 12 and submit the report to your supervisor)

Designing the Converter

2. Now, using the constraints from the previous section along with the specifications given, you will design and analyze the converter.

   (a) Analyze and dimension all of the components.

   (b) Design and optimize the power stage. This should be done in Candence.

   (c) Calculate the conduction and switching losses.

   (d) Calculate the following stress factors for each component:

   - I_{rms} (root-mean-square current)
   - $\bar{I}$ (average current)
   - V_{max} (maximum voltage)
   - $\bar{V}$ (average voltage)

   (e) Analyze and plot the current and voltage waveforms for at least one operating period in the steady-state condition.

   (f) Estimate the expected efficiency of the converter.

   Be sure to discuss your results with your supervisor before handing in your report!

(Finish above problems before June 12 and submit the report to your supervisor)

Designing the Controller

3. Sketch the schematic for the entire converter, the power stage and feedback chain,
4. Plot and comment on the Bode plots for the following characteristics
   (a) Control-to-Output transfer function
   (b) Compensation Network (if necessary)
   (c) Open Loop Gain Transfer Function
5. Simulate each of these using MATLAB.

   Be sure to discuss your results with your supervisor before handing in your report!

(Finish above problems before August 31 and submit the report to your supervisor)