A Tutorial on Robust High-Resolution Time-to-Digital Converters

Outline
- Motivation – the way to the time domain
- Basics of time-to-digital conversion (TDC)
- Delay line based TDCs
- Time-to-digital converters for sub-gate delay resolution
- Comparison of TDC concepts
- Outlook: Digital performance enhancement

Motivation
- Basic task of time-to-digital converter (TDC):
  Quantize the time interval between a start and a stop signal with a resolution of some picoseconds
- High resolution time-to-digital converters become popular for
  - Time of flight measurements
  - Phase detectors in digital PLLs
  - Measurement and instrumentation
  - High speed signal capturing, demodulators, data converters, …
- Reason for increasing popularity:
  "In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals"
  Staszewski et al. JSSC 2005
Counter Based Time Interval Measurement

- Time-to-digital converter:
  Building block converting time intervals into digital values
- Basic idea: Count cycles of known reference clock
  In fact this is not a time-to-digital converter but simply a digital counter

\[ T = T_{\text{out}} + (T - \Delta T_{\text{stop}}) - (T - \Delta T_{\text{start}}) \]
\[ T - T_{\text{out}} = \Delta T_{\text{start}} - \Delta T_{\text{stop}} \leq [T_{CP}, T_{CP}] \]
\[ 0 \leq \Delta T_{\text{start}} \leq T_{CP} \]
\[ 0 \leq \Delta T_{\text{stop}} \leq T_{CP} \]

Clock Cycle Interpolation

- Reduction of reference clock frequency possible
  \( \rightarrow \) power reduction
- Resolution increased beyond maximum frequency
Principle of Cycle Interpolation

- Propagation of start signal in delay-line is a measure for skew between start and stop signal
- Resolution limited to buffer delay
- Resolution sensitive to process and environmental variations
  - control loop for buffer delay
  - augmented resolution and digital calibration
- Robust and small,
- Nearly digital shrink factor
**TDC Converter Characteristic**

**TDC Performance Figures**

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**Alternative TDC Architectures and Sub-Gate Delay Resolution**

- Inverter delay-line
- TDC embedded in Delay Locked Loop
- Skewed parallel delay-lines
- Vernier delay-line
- Pulse shrinking technique
- Local passive interpolation technique
Inverter Delay-Line: Double Resolution

- CMOS inverter provides shortest delay available in technology
- Two delay-lines and symmetrical differential flip-flops required
- Careful layout required
- Eventually coupling between delay-lines

TDC based on Delay Locked Loop

- Controlled delay-line for absolute delay measurement
- To avoid as much analog circuitry as possible, digital calibration would be desirable
  ➔ higher resolution necessary than requested by application

Arrival Time Uncertainty along Delay Line

- Absolute arrival time variation increases along delay line (\(\sqrt{n}\))
  ➔ integral nonlinearity (INL)
- DLL operation reduces INL of delay line by \(\sqrt{n}\)
- High resolution allows for digital gain compensation
- Work mainly on monotonicity and use digital correction of nonlinearity
- Reduce length of delay line and exploit loop structure
Looped Time-to-Digital Converter

- Folding of delay line enables TDC with (theoretically) infinite dynamic range
  (in reality: intrinsic pulse shrinking gives upper limit)
- Improved linearity
- Reduced area and power consumption
- Possible for all delay-line based time-to-digital converters

Loop Control

- Stop completely async. to all other TDC signals
- One erroneous counter step causes large error in overall result
- Two fold stop signal synchronization

Alternative TDC Architectures and Sub-Gatedelay Resolution

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Parallel Scaled Delay-Line

- Sub-gated delay resolution achieved by differently sized parallel delay elements
- Strongly affected by variations
- Digital correction possible but weak linearity

\[ T_{LSB} = t_{d1} - t_{d2} \]

Not a robust concept

Vernier Delay Line-Based TDC

- Nonius principle: Race between start and stop signal in two delay lines
- Resolution given by difference of gate delays: \( T_{LSB} = t_{d1} - t_{d2} \)
- Local variations of gate delays and flip-flops limit maximum resolution to approximately 6 \( \cdot \) sigma(gate delay)
- Slow, area intensive, power hungry
- De-skewing required

Hierarchical Time-to-Digital Converter

- Significantly smaller Vernier delay-line
- Complex wiring in multiplexer introduces asymmetries, i.e. nonlinearities in the converter characteristics

Rahkonen et al., JSSC, 1993.
Dudek et al., TSSC, 2000.
**Operating principle:**
- Start and stop signals create a pulse which propagates in a line or ring of delay elements.
- Pulse width is continuously reduced by resolution time $T_{\text{conv}}$.
- Detect vanishing of pulse.

Resolution given by $T_{\text{conv}} = (T_{\text{rise}} + T_{\text{fall}} + T_{\text{fin}}} / 2$, i.e. dependent on global p/n ratio (ratioed logic!).

- Local variations of gate delays and flip-flops limit maximum resolution to approximately $6 \cdot \sigma(gate\ delay)$.
- Minimum length of un-looped delay line equal to dynamic range.
- Large non-linearity (preprocessing of pulse increases non-linearity).
- Slow, area intensive, power hungry, susceptible to variations.

**Comparison of TDC Concepts**

<table>
<thead>
<tr>
<th>Type</th>
<th>Basic</th>
<th>Vernier</th>
<th>Pulse shrinking</th>
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<tr>
<td>schematic</td>
<td><img src="image" alt="Basic schematic" /></td>
<td><img src="image" alt="Vernier schematic" /></td>
<td><img src="image" alt="Pulse shrinking schematic" /></td>
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<tr>
<td>resolution</td>
<td>$T_{\text{rise}} + T_{\text{fall}}$</td>
<td>$T_{\text{rise}} + T_{\text{fall}} + T_{\text{fin}}$</td>
<td>$T_{\text{rise}} + T_{\text{fall}} + T_{\text{fin}}$</td>
</tr>
<tr>
<td>subgate del.</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>chain/loop</td>
<td>yes / yes</td>
<td>yes / yes</td>
<td>yes / yes</td>
</tr>
<tr>
<td>$T_{\text{conversion}}$</td>
<td>$T$</td>
<td>$T_{\text{conv}}$</td>
<td>$T_{\text{conv}}$</td>
</tr>
<tr>
<td>$T_{\text{latency}}$</td>
<td>$0$</td>
<td>$T_{\text{conv}}$</td>
<td>$T_{\text{conv}}$</td>
</tr>
<tr>
<td>stage effort</td>
<td>$2 \text{ Inv} + MSFF = 6 \text{ Inv}$</td>
<td>$MSFF + 4.4 \text{ Inv} = 10.4 \text{ Inv}$</td>
<td>$MSFF + 3 \text{ Inv} = 9 \text{ Inv}$</td>
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**Principle of Local Passive Interpolation**
Linear interpolation increases the time resolution by generating intermediate signals in between two signals with the same switching direction and a skew smaller than the rise-time.
Local Passive Interpolation TDC

- Differential delay-line
- Same latency as basic TDC but increased resolution
- Linear interpolation by resistors, transistors or diodes
- Loop structure:
  - Increased dynamic range and improved linearity
- Resolution limited by local variations

Sampling of LPI Delay Line

- Fully symmetrical sense amplifier to sample differential LPI delay line
- Pre-charge eliminates history effect from prior conversion
- Coupling latches hold pseudo thermometer code while TDC is prepared for next conversion
- Post processing:
  - Bubble correction
  - Thermometer-to-binary conversion

Sizing of Interpolation Resistors

- Trade-off between power and linearity
- Low resistance:
  - large cross-current but perfect interpolation
- Large resistance:
  - small cross-currents but systematic linearity error
Characterization of TDC

- Precise time-to-digital converter measurement
  - Calibrate converter under PVT-variations
  - Required during production test

- Externally generated start and stop signals requires expensive high precision measurement equipment
  - No periodic voltage and temperature calibration
  - On-chip calibration circuitry desirable

- Generating the start and stop signal independently not feasible due to jitter
  - Derive start and stop signal from same source

- Characterization circuitry must relate the relative time interval measurement to an absolute reference

On-Chip Characterization Unit

Absolute Time Interval Reference

- Configure both delay lines as ring oscillators and count number of cycles during reference interval $T_{cal}$

\[
\frac{N_1}{T_{cal}} \quad \frac{N_2}{T_{cal}}
\]

\[
\Delta T = \frac{1}{2} T_{cal} \left( \frac{1}{N_1} - \frac{1}{N_2} \right)
\]
Converter Characteristics

Integral Non-Linearity

Differential Non-Linearity
**Single-Shot Precision**

- Variation of output data word if one time interval is measured repeatedly → caused by noise in TDC
- Limits resolution for single shot operation
- Averaging, i.e. over-sampling increases resolution

- Finite single shot precision, i.e. noise superimposes single shot measurement

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**Recommended Literature**