Mixed-Signal-Electronics

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Nyquist Rate
Digital-to-Analog Converters
Resistor String Converter
Resistor String Converter (with pass-gate decoder)

- no digital decoder
- decoder implicitly realized binary tree

\[ C_{L1} = 2C_T + C_P \]
\[ C_{L2} = 3C_T \]
\[ C_{L3} = 3C_T \]

\[ T_D = C_{L1} \left[ 3R_T + (2^W-1)R \right] + C_{L2} \left[ 2R_T + (2^W-1)R \right] + C_{L3} \left[ R_T + (2^W-1)R \right] \]
\[ T_D = \left[ 3R_T + (2^W-1)R \right] C_{ot} + 15R_T C_T + 8RC_T (2^W-1) \]
Folded Resistor String Converter

Combine the advantages of both converters:
(low effort for decoder, small load cap.)

Access scheme as in memories:
MSBs select row
LSBs select column

\[ 2^{\sqrt{2^N}} \] transistors at output bus
all bitlines are charged
Multi-Stage Resistor String Converter

- Subdivide voltage range in coarse sub-intervals first
- Copy the respective voltage interval
- Fine interpolation of the copied interval

- if opamps match the converter is monotonic
- less resistors
- reduced area and power
Binary Weighted Current Mode Converters

*Until now:* All possible voltages are generated, 1 out of $2^N$ voltages is copied to the output

$$I_F = b_1 I_r + b_2 I_r 2^{-1} + b_3 I_r 2^{-2} + b_4 I_r 2^{-3}$$

Now:

- Current mode, i.e. currents are generated, superposed and then converted into the output voltage
- Input word is already binary generated binary weighted currents and superpose them into a current that corresponds to the input word.
Monotonicity in Binary Weighted DACs

- Binary weighted converters are not necessarily monotonic
- Example:

```
1  1/2  1/4  1/8  →  6/8  1/2  1/4  1/8
1  0  0  0     0  1  1  1  →  7/8
1  0  0  0     1  0  0  0  →  7/8
```

Glitches in Binary Weighted DACs

- Different delays in the control logic of the switches cause voltage spikes, i.e. glitches

\[
\begin{align*}
0 & 1 & 1 & 1 & \rightarrow & 1 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 & \rightarrow & \uparrow & \uparrow & \uparrow & \uparrow & \rightarrow & 1 & 0 & 0 & 0 \\
0 & 1 & 1 & 1 & \rightarrow & \circ & \circ & \circ & \circ & \rightarrow & 1 & 0 & 0 & 0
\end{align*}
\]
Implementation of Binary Weighted DAC

\[ I = I_1 + I_2 + I_3 + I_4 \]

\[ I_1 = -\frac{V_{ref}}{2R} \]
\[ I_2 = -\frac{V_{ref}}{4R} \]
\[ I_3 = -\frac{V_{ref}}{8R} \]
\[ I_4 = -\frac{V_{ref}}{16R} \]

\[ V_{out} = -RF \]

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Implementation of Binary Weighted DAC

- for $b_i = 0$ the same current flows
  (not flow out to AGND)

- 30 unit resistors
- not necessarily monotonic
- glitches
- $\frac{I_{\text{max}}}{I_{\text{min}}} = \frac{R_{\text{max}}}{R_{\text{min}}} = 8 = 2^{n-1}$
Implementation of Binary Weighted DAC (with improved resistor ratio)

\[
V_{\text{out}} = V_{\text{ref}} \frac{R_F}{R} \left( 2^{-1} b_1 + 2^{-1} b_2 \right) + \frac{1}{4} V_{\text{ref}} \frac{R_F}{R} \left( 2^{-1} b_3 + 2^{-2} b_4 \right)
\]

Reference division
Implementation of Binary Weighted DAC (with improved resistor ratio)

- \( \frac{R_{\text{max}}}{R_{\text{min}}} = \frac{4K}{2R} = 2 \) (reduced)
- \( \frac{l_{\text{max}}}{l_{\text{min}}} = 8 \) (unchanged)
- Unit resistors: 19
R-2R-Ladder Network

\[ V_{ref} \]

\[ R_1, R'_1 \]
\[ R_2, R'_2 \]
\[ R_3, R'_3 \]
\[ R_4, R'_4 \]

\[ V_{ref} \]
\[ V_{ref} \]
\[ V_{ref} \]

\[ I_1 = \frac{V_{ref}}{2R} \]
\[ I_2 = \frac{V_{ref}}{2R} \]
\[ I_3 = \frac{V_{ref}}{2R} \]
\[ I_4 = \frac{V_{ref}}{2R} \]

\[ R_4' = 2R \]
\[ R_4 = 2R \parallel 2R = R \]
\[ R_3' = R + R_4 = 2R \]
\[ R_3 = 2R \parallel R_4 = R \]

\[ R_c' = 2R \]
\[ R_c = R \]
Implementation of Binary Weighted DAC (with R-2R-Ladder)

Take R-2R-ladder and replace the analog ground by a virtual ground.
Implementation of Binary Weighted DAC (with R-2R-current divider)

- R-2R ladder as current divider

\[ i = -I \left[ b_1 + 2^{-1} b_2 + 2^{-2} b_3 + 2^{-3} b_4 \right] \]

\[ R = \frac{R_1 R_2}{R_1 + R_2} \quad \Rightarrow \quad V = R i = \frac{R_1 R_2}{R_1 + R_2} I \]

\[ I_4 = \frac{R_2}{R_1 + R_2} \]

\[ I_2 = \frac{R_4}{R_1 + R_2} \]

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Switched Capacitor Amplifier
(without output reset)

\[ v_{out}[n] = -\left(\frac{C_1}{C_2}\right) v_{in}[n] \]
SC-Amplifier with Controllable Capacitors
Thermometer Code Converters (method to force monotonicity)

<table>
<thead>
<tr>
<th>#</th>
<th>binary</th>
<th>thermometer code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1 0</td>
<td>0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0 0</td>
<td>0 0 0 0 0 0 1 1</td>
</tr>
<tr>
<td>3</td>
<td>0 1 1 0</td>
<td>0 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0 0</td>
<td>0 0 0 1 1 1 1 1</td>
</tr>
<tr>
<td>5</td>
<td>1 0 1 0</td>
<td>0 0 1 1 1 1 1 1</td>
</tr>
<tr>
<td>6</td>
<td>1 1 0 0</td>
<td>0 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>7</td>
<td>1 0 1 1</td>
<td>1 1 1 1 1 1 1 1</td>
</tr>
</tbody>
</table>
Thermometer Code Converters
(method to force monotonicity)

Binary – to – thermometer code conversion

\[ \begin{align*}
\text{d}_1 & \quad \text{d}_2 & \quad \text{d}_3 & \quad \text{d}_4 & \quad \text{d}_5 & \quad \text{d}_6 & \quad \text{d}_7 \\
\text{b}_1 & \quad \text{b}_2 & \quad \text{b}_3 \\
\end{align*} \]

\[ \text{V}_{\text{ref}} \quad \text{R}_f \quad \text{V}_{\text{out}} \]
Thermometer Code Converters
(method to force monotonicity)

Top capacitors are connected to ground
Bottom capacitors are connected to $V_{\text{ref}}$
Hybrid Converter Architectures