Supply Voltages of Mixed Signal Circuits

General case: use of bipolar signals

- **VDD**: most positive potential (+2V, 4V)
- **AGND**: analog ground / reference voltage (0V, 2V)
- **VSS**: most negative potential (-2V, 0V)

Positive signals

Negative signals

Even more complex supply concepts in use → check for available voltages and definitions before starting with design.
Transistor Description (for hand calculations)

\[ I_D = \begin{cases} 
0 & \text{cut-off} \\
\frac{1}{2} \mu_C \frac{W}{L} \left[ (V_{gs} - V_{th}) \cdot V_{ds} - \frac{1}{2} V_{ds}^2 \right] & \text{linear region} \\
\frac{1}{2} \mu_C \frac{W}{L} \left( V_{gs} - V_{th} \right)^2 & \text{saturation reg}
\end{cases} \]

Subthreshold current

\[ I_D = \mu_C \frac{W}{L} (\eta - 1) V_T^2 \exp \left( \frac{V_{gs} - V_{th}}{2V_T} \right) \cdot \left[ 1 - \exp \left( -\frac{V_{ds}}{V_T} \right) \right] \]

\[ V_{gs} - V_{th} < 0 \]
\[ 0 < V_{gs} - V_{th} > V_{ds} \]
\[ V_{gs} - V_{th} < V_{DS} \]

\[ \beta = \mu C \frac{W}{L} \]
MOS Transistor as Switch

linear region

\[ I_D = \beta_n \left( (V_{gs} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right) \]

\[ C_{IN} = \frac{I_D}{V_{DS}} = \beta_n (V_{gs} - V_{TH}) = \beta_n (V_{DD} - V_{Signal} - V_{TH}) \]

PMOS conductance

\[ V_{Signal} < V_{DD} - V_{TH} \]

\[ C_{IP} = -\beta_p (V_{gs} - V_{TP}) = -\beta_p (V_{SS} - V_{Signal} - V_{TP}) \]

\[ V_{Signal} > V_{SS} - V_{TP} \]

Pros:

Transmission gate

Conductance $G$

Pros:

\[ V_{SS} \rightarrow V_{TP} \]

\[ V_{DD} \rightarrow V_{Signal} \]
Chapter 2

Sample and Hold Circuits
Sample & Hold Circuit
Sample & Hold Circuit (cont)

1. Finite rise-time / finite bandwidth due to RC constant
2. Amplifier dynamics
   (finite settling time, overshoot, ringing)
Sample & Hold: Clock Feed-Through

3. Clock feed-through due to capacitive coupling.

\[ \Delta V_{out} = \frac{C_p}{C_p + C_v} \Delta V_{in} \]
\[ \Delta V_{in} = V_{DD} - V_{SS} \]
4. Charge Injection: mobile carriers are removed

\[ \Delta Q = \frac{1}{2} \cdot W \cdot L \cdot \frac{\varepsilon_0 \varepsilon_{dia}}{t_{ox}} (V_{gs} - V_{th}) \]

\[ \Rightarrow \Delta V_{out} = \frac{1}{C_v} \Delta Q \]

1:1 distribution is an approximation for fast switching
Sample & Hold Circuit (cont)

5. 

6. Clock jitter
7. Droop in hold mode: leakage currents discharge hold cap
8. Linearity
S&H Output Signal

Overshoot and settling time
S/H output within specified tolerance
Droop and feedthrough
Pedestal error
Output slewing

$V_{IN}^{max}$

Acquisition time
Hold mode
Sample command issued
Hold command issued

$v_{IN}$
$v_{OUT}$
Impact of Jitter on S&H Performance

Consider a sinusoidal signal \( v(t) = A \cdot \sin(\omega t) \)

Signal power \( \overline{v^2} = \frac{1}{2}A^2 \)

Rate of change \( \frac{dv}{dt}(t) = A\omega \cdot \cos(\omega t) \)

Jitter = random variation of sampling instance

\[
t_s = nT + \Delta t_n
\]

\[
p\Delta t = \frac{1}{\sqrt{2\pi\sigma}} \exp\left(-\frac{\Delta t^2}{2\sigma^2}\right)
\]

Sampling error:

\[
\Delta v = \frac{dv}{dt} \Delta t = A\omega \cdot \cos(\omega t) \Delta t
\]
Impact of Jitter on S&H Performance

Noise power resulting from sampling error

\[ \Delta v^2 = \int_{0}^{T} \int_{-\infty}^{\infty} A^2 \omega^2 \cdot \cos^2 (\omega t) \Delta t^2 \cdot p_{\Delta t} p_t d(\Delta t) dt \]

\[ p_t = \frac{1}{T} \quad p_{\Delta t} = \frac{1}{\sqrt{2\pi}\sigma} \exp \left( -\frac{\Delta t^2}{2\sigma^2} \right) \]

\[ \Delta v^2 = A^2 \omega^2 \int_{-\infty}^{\infty} \Delta t^2 p_{\Delta t} d\Delta t \cdot \frac{1}{T} \int_{0}^{T} \cos^2 (\omega t) dt = \frac{1}{2} (A\omega \sigma)^2 \]

Signal-to-Noise Ratio \[ SNR = 10 \lg \frac{\frac{1}{2} A^2}{\frac{1}{2} (A\omega \sigma)^2} = 20 \lg \frac{1}{\omega \sigma} \]

→ maximum achievable SNR for given jitter

→ frequency dependent, i.e. the larger the bandwidth the higher the clock requirements
Impact of Offset-Voltage

- Offset voltage of opamp is modeled as voltage source in series to input terminal
- Offset voltage is directly visible at output terminal

\[ V_{out} = V_v - V_o \]
S&H with Correlated Double Sampling

Phase 1: Tracking Phase

Opamp acts as voltage follower

\[ V_{out} = V_0 \]

\[ V_C = V_{in} - V_0 \]

Phase 2:

Separate cap from input and put it in feedback of opamp

\[ V_{out} = V_C + V_0 \]

\[ = V_{in} - V_0 + V_0 \]

\[ V_{out} = V_{in} \]
Noise in Discrete Time Systems

Noise is a random process → statistical description is required

- time domain: noise signal $a(t)$

$$\bar{a} = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} a(t) \, dt = 0$$

$$\bar{a^2} = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} a^2(t) \, dt \neq 0$$

- frequency domain: power spectral density

$$\bar{a^2} = \int_{0}^{\infty} psd(f) \, df$$
Noise of Sampled Signals
– kT/C-Noise –

\[
\frac{1}{1+SRC}
\]

\[
\frac{4KTR}{1+4\pi^2 R^2 C^2 f^2}
\]

\[
\frac{KT}{C}
\]

Remarks:
- Sampling makes this a little bit more complicated as noise is a wide band signal so there is aliasing of replica spectra. However, the noise power in the baseband is still kT/C
- This is only a lower bound of noise power, buffers contribute also to overall noise power
Closed Loop Track & Hold Circuit 1

- Basic sampling circuit is embedded in feedback loop
  - Very high input impedance
  - Reduction of non-idealities (e.g. buffer offset) by loop gain
  - Loop must be designed stable → speed degradation
  - Feedback is broken during hold mode
    - Input opamp saturates
    - Long slewing time when circuit returns to track mode

offset not canceled

not critical wrt. offset errors
Closed Loop Track & Hold Circuit 2

- Hold mode:
  Input opamp is configured as voltage follower
  → fast settling when circuit returns to track mode
Closed Loop Track & Hold Circuit 3

- Storage capacitor is shifted to feedback loop of output amplifier (integrator)
  - Swing across switch is always near to AGND
  - Error injection becomes nearly signal independent (pedestal error)
  - No appertur jitter

- Input opamp is grounded during hold phase
  - fast settling when switched to track mode
  - signal feedthrough is minimized

- Reduced speed due to stability requirements
Closed Loop Track & Hold Circuit 4

- Additional error replica to avoid the pedestal error
Sample & Hold Circuits

- charge injection
- apperture jitter
- linearity
- offset voltages
- noise

Sample & Hold Circuit

- finite bandwidth
- clock feed-throug
- clock jitter
- buffer dynamics (settling)
- leakage (droop)